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10/798,482	03/12/2004	Akira Takahashi	OKI 414	6303

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EXAMINER	
KRAIG, WILLIAM F	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,482	TAKAHASHI, AKIRA	
	Examiner	Art Unit	
	William Kraig	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☒ Claim(s) *6 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1 and 3 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. A limitation of both claims is that the non-doped polysilicon is "contiguous to at least one of the N type polysilicon gate and the P type polysilicon gate". Fig. 3 (a and b) of the instant application both show a "region...for forming a...transistor gate". The transistor gates formed from those regions can be seen in Fig 3(c). Nowhere in the drawings or in the specification does it ever describe the non-doped polysilicon being contiguous to either the P type or N type *"gate"*.

2. Claims 2 and 4-11 rejected under 35 U.S.C, first paragraph, as being dependent therefrom.

3. Claims 1-3 and 6-11 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear whether the limitation "polysilicon gate" is referring to the actual gate structure that is formed by the etching (later claims indicate that it is not) or the polysilicon layer out of which the gate structure is formed. For purposes of this office action the Examiner will assume that the applicant is referring to the polysilicon layer that the gate structures are formed out of and will examine the claim as such. The examiner recommends that the claim be rewritten so that the meaning of the limitation "polysilicon gate" is distinct.

4. Claims 4 and 5 rejected under 35 U.S.C. second paragraph, as being dependent therefrom.

Claim Objections

5. Claim 2 objected to because of the following informalities. The examiner is unsure what the term "phosphor" refers to. The examiner believes that the term "phosphor" is meant to read --phosphorus-- and will examine the claim as such. Appropriate correction is required.

6. Claim 6 objected to because of the following informalities: The examiner believes that the term "on" is misused in this case and should be replaced with --out of-- or the equivalent. Appropriate correction is required.

7. Claim 9 objected to because of the following informalities: The examiner believes that the term "on" is misused in this case and should be replaced with --out of-- or the equivalent. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 3, and 6-11 rejected under 35 U.S.C. 102(e) as being anticipated by Gabriel et al. (U.S. Patent # 6541359).

Regarding claim 1, Fig. 5A of Gabriel et al. discloses a semiconductor device comprising:

a region for forming an N type polysilicon gate (540) and a region for forming a P type polysilicon gate (540) (Col. 6, Line 62 – Col. 7, Line 9), both

disposed simultaneously (both disposed as part of gate electrode layer (310)), together occupying a first total area (twice the area of doped portion (540) – for forming both an N type and a P type gate); and

non-doped polysilicon (560a) disposed contiguous to at least one of the region for forming the N type polysilicon gate and the region for forming the P type polysilicon gate (540), the non-doped polysilicon (560a) occupying a second area (area of unimplanted portion (560a)) larger than the first total area (twice the area of doped portion (540) – for forming both an N type and a P type gate) of the regions for forming the N type and P type polysilicon gates (the area of the non-doped polysilicon (560a) (also 560b) can be seen to be greater than twice the area (for forming both an N type and a P type gate) of doped portion (540)).

Regarding claim 3, Fig. 5A of Gabriel et al. discloses a dry etching method (Col. 1, Lines 34-38) for a semiconductor device, comprising the following steps of:

simultaneously gate-etching a region for forming an N type polysilicon gate (540) and a region for forming a P type polysilicon gate (540) (Col. 6, Line 62 – Col. 7, Line 9); and

setting an etching area (area of unimplanted portion (560a)) occupied by non-doped polysilicon (560a), which is contiguous to at least one of the region for forming the N type polysilicon gate and the region for forming the P type polysilicon gate (540), larger than a total area (twice the area of doped portion (540) – for forming both an N type and a P type gate) of the region for forming

the N type polysilicon gate and the region for forming the P type polysilicon gate (the area of the non-doped polysilicon (560a) (also 560b) can be seen to be greater than twice the area (for forming both an N type and a P type gate) of doped portion (540)).

Regarding claim 6, Fig. 5A of Gabriel et al. discloses the semiconductor device according to claim 1, comprising gate electrodes (550) formed out of the region for forming the N type polysilicon gate (540) and the region for forming the P type polysilicon gate (540) (Col. 6, Line 62 – Col. 7, Line 9) by polysilicon gate etching (Col. 6, Line 62 – Col. 7, Line 9).

Regarding claim 7, Fig. 4 of Gabriel et al. discloses the semiconductor device according to claim 6, wherein the gate electrodes (355) are smaller in area than the region for forming the N type polysilicon gate (465a) or the region for forming the P type polysilicon gate (450) (Col. 6, Lines 12-20).

Regarding claim 8, Fig. 5A of Gabriel et al. discloses the semiconductor device according to claim 1, comprising a plurality of the region for forming the N type polysilicon gate (540) and the region for forming the P type polysilicon gate (540) disposed in mixed form (Col. 6, Line 62 – Col. 7, Line 9).

Regarding claim 9, Fig. 5A of Gabriel et al. discloses the dry etching method (Col. 1, Lines 34-38) according to claim 3, wherein the step of simultaneously gate-etching the region for forming the N type polysilicon gate (540) and the region for forming the P type polysilicon gate (540) comprises polysilicon gate etching (Col. 6, Line 62 – Col. 7, Line 9) to form gate electrodes (550) out of the region for forming the N type polysilicon gate (540) and the P type polysilicon region (540) (Col. 6, Line 62 – Col. 7, Line 9).

Regarding claim 10, Fig. 4 and Fig. 5A of Gabriel et al. disclose the dry etching method (Col. 1, Lines 34-38) according to claim 9, wherein the gate electrodes (355) are smaller in area than the region for forming the N type polysilicon gate (465a) or the region for forming the P type polysilicon gate (450) (Col. 6, Lines 12-20).

Regarding claim 11, Fig. 5A of Gabriel et al. discloses the dry etching method (Col. 1, Lines 34-38) according to claim 3, comprising forming a plurality of the region for forming the N type polysilicon gate and the region for forming the P type polysilicon gate disposed in mixed form (Col. 6, Line 62 – Col. 7, Line 9).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Gabriel et al.

Regarding Claim 2, Gabriel et al. discloses N-type and P-type polysilicon gates (Col. 6, Line 62 – Col. 7, Line 9), and the claimed impurities of boron and phosphor are commonly used materials in the semiconductor art to determine the conductivity, P or N, of conductive layers and thus would have been obvious to the ordinary artisan.

10. Claims 4 and 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Gabriel et al. in view of Lee et al. (U.S. Patent # 5665203).

Regarding Claims 4 and 5, Gabriel et al. discloses the dry etching method (Gabriel et al., Col. 1, Lines 34-38) according to claim 3, wherein the etch includes a stage using a mixed gas of HBr and 0_2 (Gabriel et al., Col. 1, Lines 63-65), but fails to disclose the gate etching process being a two-step process, wherein the second step is a stage using a mixed gas of HBr, 0_2 and He.

Lee et al. teaches a similar method wherein the gate etching process is a two-step process which uses a first stage atmosphere of HBr, Cl_2 and He and a second stage atmosphere of HBr, 0_2 and He (Lee et al., Col. 2, lines 39-41).

It would have been obvious to one of ordinary skill in the art to incorporate the method of Lee et al. into the method of Gabriel et al. The ordinary artisan would have

been motivated to modify Gabriel et al. in the above manner for the purpose of forming perfectly vertical gate sidewalls (Lee et al. Col. 2, Lines 23-28)

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tzeng et al. (U.S. Patent # 6376294), Liu et al. (U.S. Patent # 6429067) and Huang (U.S. Patent # 6117723) all disclose similar semiconductor devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFK

GEORGE ECKERT
PRIMARY EXAMINER